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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,206	10/09/2003	Mototsugu Fuji	HITA.0441	8330

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EXAMINER	
JACOB, MARY C	
ART UNIT	**PAPER NUMBER**
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/681,206	FUJI ET AL.	
	Examiner	Art Unit	
	Mary C. Jacob	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2 and 4-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2 and 4-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The response filed 7/11/07 has been received and considered. Claims 2, 4-9 are presented for examination.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/11/07 has been entered.

Drawings

3. The objections to the drawings recited in the 3/13/07 Office Action still apply. The Examiner acknowledges Applicant's response that new drawings will be filed when it is determined that allowable claims are present in the application.

Specification

4. The objections to the specification recited in the 3/13/07 Office Action still apply. The Examiner notes Applicant's response that a new specification will be filed when it is determined that allowable claims are present in the application.

Claim Objections

5. The objections to the claims recited in the Office Action dated 3/13/07, not repeated below, have been withdrawn in response to the amendments to the claims filed 7/11/07.

6. Claim 1 is objected to because of the following informalities: line 31 recites, "designed logic circuit one said device", it should read, "designed logic circuit on said device. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The rejections of the claims under 35 U.S.C. 112, second paragraph, recited in the Office Action dated 3/13/07 have been withdrawn in response to the amendments to the claims filed 7/11/07.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 4-8 are rejected under 35 U.S.C. 103(a) as being obvious over Evans et al (US Patent 6,279,146) in view of Fuji et al (US Patent 6,564,367).

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. As to Claim 2, Evans et al teaches: a logic simulation accelerator (column 3, lines 63-66; column 8, line 67-column 9, line 3; column 9, lines 60-67; column 10, lines 18-24) including: a logic simulator operating on a general purpose processor to logically verify operational correctness of a designed logic circuit (Figure 2, element 86, 118); a device which includes a programmable FPGA module composed by FPGAs to be programmed to physically realize functions of the designed logic circuit (Figure 2, element 60 and included elements; column 9, lines 3-11) which is mounted to the logic simulator via a connector (column 9, lines 29-35; column 8, lines 44-49); a bridge circuit which is mounted to the logic simulator and which selectively transmits and receives corresponding data between said general purpose processor and said device (Figure 2, element 72; column 9, lines 29-63); wherein the verification logic for verifying said designed logic circuit implemented on said device provides a means for transmitting a direction control signal which controls a transmission direction of two-way signals between said FPGA module and said bridge circuit thereby performing logic verification of the designed logic circuit by the logic simulator in parallel with physical realization of the designed logic circuit on said device, and said direction control signal is sent to the

bridge circuit via one of said two-way signals (column 8, line 67-column 9, line 3; column 9, lines 37-43; column 10, line 61-column 11, line 8; column 13, lines 6-9; lines 25-28; column 14, lines 13-25; Figure 5).

11. Evans et al does not expressly teach: wherein all the pins of the FPGA module are wired directly to the bridge circuit via the connector; wherein a cutting end of a verification logic which verifies said designed logic circuit realized on said device is assigned to the connector of the FPGA module for accelerating logic simulation; wherein a correspondence between each of said all pins of said FPGA module and a logic signal from said general purpose processor is established on said logic simulator.

12. Fujii et al teaches a logic dividing and module wiring system that allows for logic emulation to be carried out at a high speed (column 4, line 66-column 5, line 11) wherein the system contains FPGA devices implementing logic for verification (column 3, lines 61-64; Figure 3; Figure 6, "Type A" and description), a module connector for electrically connecting the module to an external device (column 3, lines 66-67; Figure 6 and description), wherein all the pins of the FPGA module are wired directly to the connector (column 4, line 66-column 5, line 11); wherein a cutting end of a verification logic which verifies said designed logic circuit realized on said device is assigned to the connector of the FPGA module for accelerating logic simulation (column 4, line 66-column 5, line 11; column 6, lines 64-66; column 7, lines 44-48); wherein a correspondence between each of said pins said FPGA module and a logic signal from said general purpose processor is established on said logic simulator (column 7, lines 44-48; Figure 5 and description).

13. Evans et al and Fujii et al are analogous art since they are both directed to accelerating logic operations that verify a logic design programmed a plurality FPGAs wherein the module containing the FPGA devices is connected to an external device.

14. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the logic verification system as taught by Evans et al to further include the direct wiring of the FPGA module to the bridge circuit like the direct wiring of the FPGAs to the connector, wherein a cutting end of a verification logic of said designed logic circuit is assigned to the connector of the FPGA module and establishing a correspondence between each pin of the pins of said FPGA module and a logic signal on the logic simulator as taught in Fujii et al, since Fujii et al teaches a logic dividing and module wiring system that allows for logic emulation to be carried out at a high speed (column 4, line 66-column 5, line 11).

15. As to Claim 4, Evans et al in view of Fujii et al teach: the logic verification system further comprising means for automatically detecting a signal direction of a two-way signal between said FPGA module and the bridge circuit (Evans: column 5, lines 40-56; column 13, lines 25-28), and the program data of the same FPGA module implementing different verification logics used in verification processes consisting of acceleration of logic simulation and logic emulation for a plurality of designed logic circuits (Evans et al: column 8, line 66-column 9, line11; column 10, lines 18-24; Fujii et al: Figure 1, element 101; column 4, line 66-column 5, line 9).

16. As to Claims 5 and 7, Evans et al in view of Fujii et al teach: wherein said means for automatically detecting the signal direction of the two way signal sets a drivability

level of output circuits of the FPGA module and the bridge circuit and giving a priority in determination of signal direction to one of the FPGA module and the bridge circuit which has a higher drivability (Evens et al: column 5, lines 40-47; column 13, lines 25-28; column 13, line 47-column 14, line 25).

17. As to Claim 6, Evans et al in view of Fujii et al teach: means for inputting the signal direction of the two-way signal to the logic simulator on the general purpose processor, wherein a disagreement between the signal direction of the two-way signal to the logic simulator and a signal direction indicated in said direction control signal is detected by comparing said signal directions (Evans et al: column 13, lines 25-28; column 14, lines 26-49).

18. As to Claim 8, Evans et al in view of Fujii et al teach: wherein said direction control signal is added into the verification logic (Evans et al: column 11, lines 58-66; column 12, lines 31-34; column 14, lines 12-25; Fujii et al: column 8, lines 25-27).

19. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Evans et al in view of Fujii et al as applied to claim 2 above, and further in view of Quayle et al (US Patent 6,694,464).

20. Evans et al in view of Fujii et al teach a logic verification system that includes means for transmitting a direction control signal between said FPGA module and said bridge circuit.

21. Evans et al in view of Fujii et al do not expressly teach: wherein said direction control signal is instead transmitted on a time division basis with said two-way signals.

22. Quayle et al teaches a hardware emulation system which reduces hardware cost by time-multiplexing multiple design signals onto physical logic chip pins and printed circuit board traces but which does not have the limitations of low operating speed and poor asynchronous performance (column 4, lines 7-12) wherein the hardware emulation system includes a plurality of reprogrammable logic devices and programmable input/output terminals (column 4, lines 23-31), wherein a direction control signal is transmitted on a time division basis with two-way signals (Figure 6, element 80; column 11, lines 20-24, 33-37, 42-54).

23. Evans et al in view of Fujii et al are analogous art since they are directed to hardware emulation systems that use reprogrammable logic devices verify a logic design and improve performance of the emulation system.

24. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the transmission of a direction control signal as taught by Evans et al in view of Fujii et al to include the transmission of the direction control signal on a time division basis with said two-way signals as taught in Quayle et al since Quayle et al teaches a hardware emulation system which reduces hardware cost by time-multiplexing multiple design signals onto physical logic chip pins and printed circuit board traces but which does not have the limitations of low operating speed and poor asynchronous performance.

Response to Arguments

25. Applicant argues that the examiner admits that Evans does not teach, "all pins of the FPGA module being directly wired to the bridge circuit, a cutting end of a verification logic of said one of the plurality of designed logic circuits is assigned to an external interface connector of the FPGA module, and a correspondence between each pin of the external interface connector of said FPGA module and a logic signal is established on said logic simulator on said general purpose processor" (page 8, paragraph 2). The Examiner contends that the teachings of Fujii et al are relied upon to teach or suggest these limitations as recited above.

26. Applicant argues that Evans executed emulation on its own, rather than "in parallel with logic verification of the designed logic circuit" (page 8, paragraph 3). The Examiner would like to point out that Evans teaches that the developer uses the GUI to "divide the target system design between a portion that is to be simulated by a simulation program (86) and that which resides within the verification engine (60) (column 8, line 67-3)". The Examiner contends that this teaching of Evans shows that the emulation taking place in verification engine (60) is running in parallel with logic verification of the designed logic circuit by simulation program (86).

27. Applicant argues that Evans does not provide means for transmitting a direction control signal which controls a transmission direction of two-way signals between said FPGA module and said bridge circuit directly connected to all pins of the said FPGA module (page 8, paragraph 3). The Examiner contends that the combined teachings of Evans et al in view of Fujii et al, not Evans alone, are relied upon to teach or suggest,

"all pins of the FPGA module wired directly to the bridge circuit" as recited above. As for the "means for transmitting a direction control signal which controls a transmission direction of two-way signals between said FPGA module and said bridge circuit", Evans teaches bridge circuit (Figure 2, element 72) which enables communication between the simulation program (6) and the FPGA module (verification engine (60)). This bridge circuit communicates with the FPGA module through the "phoneme recognition bus wrap FPGA" (84) and the rave time multiplexed bus (110) (column 9, lines 44-56). The communication between the bridge circuit and the FPGA module occurs through bus wrap (84) which provides the means for transmitting a direction control signal to control a transmission direction of two-way signals between the FPGA module and the bridge circuit (column 10, line 61-column 11, line 8; column 13, lines 6-9; lines 25-28; column 14, lines 13-25; Figure 5) wherein a direction control signal controls whether the bus wrapper will drive pin 147 (Figure 5) of the bridge circuit, or whether the pin 147 of the bridge circuit will drive the bus data line 144.

28. Applicant argues that Fujii also executes emulation on its own rather than "in parallel with logic verification of the designed logic circuit" (page 8, paragraph 4). The Examiner contends that the teachings of Evans et al are relied upon to teach or suggest this limitation as discussed above. However, Fujii et al also teaches, "the present invention presents a logic emulation system" (column 4, lines 18-20) wherein logic emulation is performed (Figure 25, step S2505) and "in logic emulation, a logic circuit to be verified is programmed by using an FPGA and logic of the circuit is verified by actually operating the FPGA in conjunction with an actual product sold in the market or

an existing LSI" (column 1, lines 37-40). This verification of the logic circuit by operating the FPGA in *conjunction with* an actual product or existing LSI teaches that emulation is performed in parallel with logic verification of a designed logic circuit.

29. Applicant argues that Fujii et al does not provide "means for transmitting a direction control signal which controls a transmission direction of two-way signals..." thereby performing the parallel logic verification scheme (page 8, paragraph 5). The Examiner contends that Evans et al teaches or suggests this "means for transmitting a direction control signal" and the "parallel logic verification" as discussed above. The Examiner contends that the combined teachings of Evans et al in view of Fujii et al, not Evans alone, are relied upon to teach or suggest "all pins of the FPGA module wired directly to the bridge circuit" as recited above

30. Applicant recites that the features in claims 4-9 are absent from the disclosures of Evans et al or Fujii et al, however, fails to set forth how the language of the claims distinguishes them from the references. The Examiner asserts that the combined teachings of Evans et al and Fujii et al teach or suggest the limitations of claims 4-9 as recited above.

Conclusion

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

32. Hsieh et al (US Patent 5,426,738) teaches external access to a field programmable circuit board is provide through an array of field programmable interconnect devices which

include signal buffers that automatically sense the direction of flow of bi-directional signals and bugger the signals in the appropriate direction.

33. Graves et al (US Patent 5,946,472) teaches high speed sequential modeling in a simulator or emulator environment wherein a sequential control system executes multiple commands during each emulation cycle so that the concurrent operations model within the accelerator/emulator and the sequential operations model within the sequential control system achieve a high degree of parallel operation, greatly enhancing system speed and performance.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C. Jacob whose telephone number is 571-272-6249. The examiner can normally be reached Tuesday-Thursday, 7AM-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary C. Jacob
Examiner
AU2123

MCJ
9/5/07

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